# AND8247/D

# Application Note for a 5.0 to 6.5 W POE DC to DC Converter

**Prepared by: Frank Cathell**
ON Semiconductor

**ON Semiconductor®**

**http://onsemi.com**

**APPLICATION NOTE**

## INTRODUCTION

A solution to one aspect of Power Over Ethernet (POE) is presented here utilizing the ON Semiconductor NCP1031 series of monolithic, high voltage switching regulators with internal MOSFET. The application note provides details for constructing an inexpensive, high efficiency, 5.0 V DC power supply with a power output of 5.0 to 6.5 W, (output power is conversion mode dependent — see DC to DC Converter Operation description below). The associated input circuitry for responding to POE detection and classification protocol is also included. ON Semiconductor also can provide a demonstration PC board with this circuitry upon request.

### POE Background

As a result of IEEE Standard 802.3AF, it is now possible to inject DC power through Ethernet data transmission lines to power Ethernet communication devices as long as the end power requirement is less than 13 W. The parametric details of DC power transmission and the associated terminology is outlined in this IEEE document. POE consists of two power entities: Power Sourcing Equipment (PSE) and Powered Devices (PDs). The PSEs typically provides 48 Vdc nominal to the LAN cables while the PDs are small DC−DC converters at the load end of the cables which transform the 48 V to logic levels such as 5.0 Vdc or 3.3 Vdc or both, to power the communications equipment. The PDs should be able to operate with a maximum average input power of 12.95 W, and should be able to tolerate an input voltage range of 36 to 57 Vdc. In addition, a certain “protocol” is required in which the PD is detected (Signature Mode) and then classified (Classification Mode) according to its maximum power level.

**Signature Detection:** The upstream PSE equipment detects the PD by injecting two different voltages between 2.8 and 10 Vdc into the PD input terminals. If the detected impedance of the PD as measured by the V/I slope is above 23.7 KΩ, and below 26.25 KΩ, the PD is considered present. If the impedance is less than 15 K, or greater than 33 K, the PD is considered not present, and no further voltage will be applied.

**Classification Mode:** To classify the PD according to its intended power level, the PSE will again source a voltage between 14.5 and 20.5 Vdc to the PD. The classification is determined by the current drawn by the PD upon application of this voltage, and is summarized in the following table:

| Class | $P_{min}$ | $P_{max}$ | $I_{class\ min}$ | $I_{class\ max}$ | $R_{class}$ (R4) |
|---|---|---|---|---|---|
| 0 | 0.44 W | 12.95 W | 0 mA | 4.0 mA | Open |
| 1 | 0.44 W | 3.84 W | 9.0 mA | 12 mA | 217 Ω |
| 2 | 3.84 W | 6.49 W | 17 mA | 20 mA | 135 Ω |
| 3 | 6.49 W | 12.95 W | 26 mA | 30 mA | 91 Ω |
| 4 | TBD | TBD | 36 mA | 44 mA | 62 Ω |

Note that from the 4th and 5th columns on the table, that the current drawn from the PSE falls between the $I_{class}$ minimum and maximum values for a given power classification. The last column is the value of the resistor (R4) required for classification in the circuit described by this application note.

### Additional Input Features

In addition to the signature and classification circuitry, the PD must also include circuitry to limit the inrush current from the PSE to 400 mA when the input voltage is applied, and to prevent any quiescent currents or impedances caused by the DC−to−DC converter to be ignored during the signature and classification processes.

### Signature/Classification Circuit Details

Referring to the schematic of Figure 2, the input signature and classification circuitry is designed around a few discrete and inexpensive ON Semiconductor parts that include the TL431 programmable reference, a 2N7002 signal level MOSFET, a 2N5550 NPN transistor, an NTD12N10 MOSFET and several Zener diodes and a few resistors and capacitors. For signature detection, a 24.9 K resistor (R1) is placed directly across the input. Note that during signature detection, the input voltage is below 10 V and the constant current source formed by U1, Q2 and R4 is off because of the 9.1 V Zener that must be overcome to bias this circuit. Note also that MOSFET Q3, which functions as a series input switch in the return leg of the DC−DC converter, will be off until the input voltage exceeds approximately 27 V. This voltage is the sum of D2's Zener voltage and the gate threshold of Q3.

As the voltage is ramped up to the classification level, D1 conducts above approximately 9.8 V and the current source formed by U1, Q2 and resistor R4 turns on and the current is precisely limited by the reference voltage of U1 (2.5 V) and the classification resistor R4.

Once classification is verified the input can now ramp up to the nominal 48 V. Once this voltage exceeds the sum of Q3's gate threshold and D2's Zener voltage, Q3 will start to turn on. It will not turn on abruptly, however, but will operate in its linear region momentarily due to the RC time constant created by R6 and C2. The momentary operation in the linear region allows for inrush current limiting because Q3 will act like a resistor during this period. D3 clamps the voltage on Q3's gate to 15 V, while R5 provides a discharge path for C2 when the input from the PSE is off. MOSFET Q1 will also turn on at the same voltage level as Q3, and this will switch off the U1/Q2 current source so as to reduce additional current drain from the input.

### DC to DC Converter Operation

The DC−to−DC converter is designed around ON Semiconductor's monolithic NCP1031 switching regulator IC (U2). For a 5.0 W maximum output, the converter is configured as a discontinuous mode (DCM) flyback topology with the conventional TL431 and optocoupler voltage feedback scheme. Modifications to the transformer design and the control loop compensation network for continuous conduction mode flyback operation will allow up to 6.5 W (1.3 A) output. The input utilizes a differential mode pi filter comprised of C3, L1 and C4. Control chip startup is accomplished when the undervoltage terminal at pin 6 exceeds 2.5 V. The resistor divider network of R7, R8, and R9 sets the chip's under and overvoltage levels to 35 and 80 V, respectively. Internal startup bias is provided thru pin 8, which drives a constant current source that charges $V_{cc}$ capacitor C7. Once U2 has started, the auxiliary winding on transformer T1 (pins 2, 3) provides the operating bias via diode D4 and resistor R11.

Voltage spikes caused by the leakage inductance of T1 are clamped by the network of C5, D6 and R10. The actual power rating on R10 will be a function of the primary−to−secondary leakage inductance of T1, and the lower the better. Capacitor C6 sets the switching frequency of the converter to approximately 220 kHz.

Because of the required secondary isolation, a TL431 (U4) is implemented as an error amplifier along with optocoupler U3 to create the voltage sensing and feedback circuitry. The internal error amplifier in U2 has been disabled by grounding pin 3, the voltage sense pin, and the amplifier's output compensation node on pin 4 is utilized to control the pulse width via the optocoupler's photo transistor. The output voltage sense is divided down to the 2.5 V reference level of the TL431 by R16 and R17, and closed loop bandwidth and phase margins are set by C9 and R15 for DCM operation. Additional components C14, C15 and R12 are required for feedback loop stabilization if configured for CCM flyback operation. C8 on the primary side provides noise decoupling and additional high frequency roll off for U2. This implementation provides output regulation better than 0.5% for both line and load changes, and a closed loop phase margin of better than 50°.

Output rectifier D5 is a three amp Schottky device for enhanced efficiency, and the output voltage is filtered by the pi network comprised of C11, L2 and C12. Typical peak−to−peak noise and ripple on the output are below 100 mV under all normal load and line conditions. C13 provides for additional high frequency noise attenuation. Typical input to output efficiency is in the area of 75% at full load. Higher efficiencies can be achieved by replacing D5 with a MOSFET based synchronous rectifier circuit (see ON Semiconductor application note, AND8127, for implementing a simple synchronous rectifier circuit to a flyback topology).

Overcurrent protection is provided by the internal peak current limit circuit in the NCP1031. The circuit can provide a continuous output current of 1.3 A at 25°C with surge up to 1.5 A when configured as a CCM flyback before overcurrent and/or overtemperature limiting ensues. When configured for the discontinuous mode, the current is limited to about 1.0 A with a 1.2 A peak.

## Magnetics Design

The discontinuous mode flyback transformer design is detailed in Figure 3 and the continuous mode transformer is shown in Figure 4. In the design of flyback transformers, it is essential to keep the windings in single layers and evenly spread over the window length of the core structure to keep leakage inductance minimized. In this application, this was easily achieved, with a small EF16 ferrite core from Ferroxcube.

## Discontinuous Versus Continuous Mode Operation

In discontinuous mode flyback operation, the inductor current falls to zero before the MOSFET switch is turned on again. This mode of operation causes the output to have a first order filter network characteristic and, as a consequence, feedback loop stabilization is simple and wide bandwidth for good output transient response can be achieved. This operational mode, unfortunately results in higher peak switch currents and limits the power output of this circuit due to the internal current limit set point and the thermal protection circuits in the NCP1031. With continuous current mode operation, where the MOSFET can turn back on before the inductor current is zero, the peak switch current is less, so higher power outputs can be achieved without overcurrent protection intervention. There is a cost, however, to this latter mode of operation in that the control loop bandwidth must be made lower with a resulting poorer transient response to load and line variation. CCM operation introduces a right half−plane zero to the power topology response characteristic which may need to be compensated for with the additional feedback components shown in Figure 2, if proper feedback stability is to be achieved. CCM may also generate more EMI due to the fact that the output rectifier must now be force commutated off.

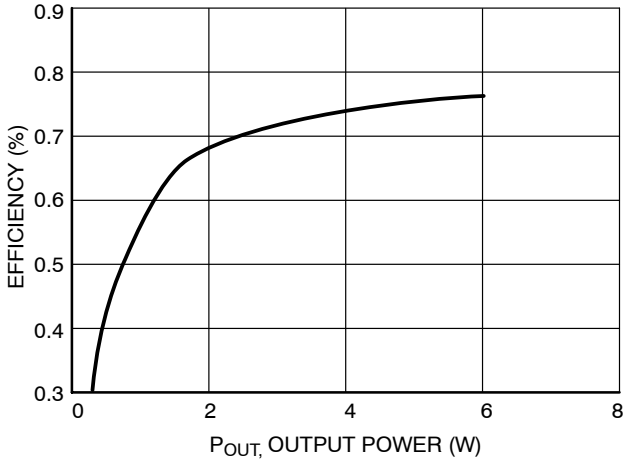



**Figure 1. Efficiency Versus Output Power Graph**

## References

1. IEEE Standard 802.3AF (Ethernet power transmission standards).
2. Power Electronic Technology Magazine, June 2004, Page 45.
3. ON Semiconductor Data Sheet – NCP1030, NCP1031.
4. On Semiconductor Application Note AND8119, “Design of an Isolated 2.0 W Bias Supply for Telecom Systems Using the NCP1030”.

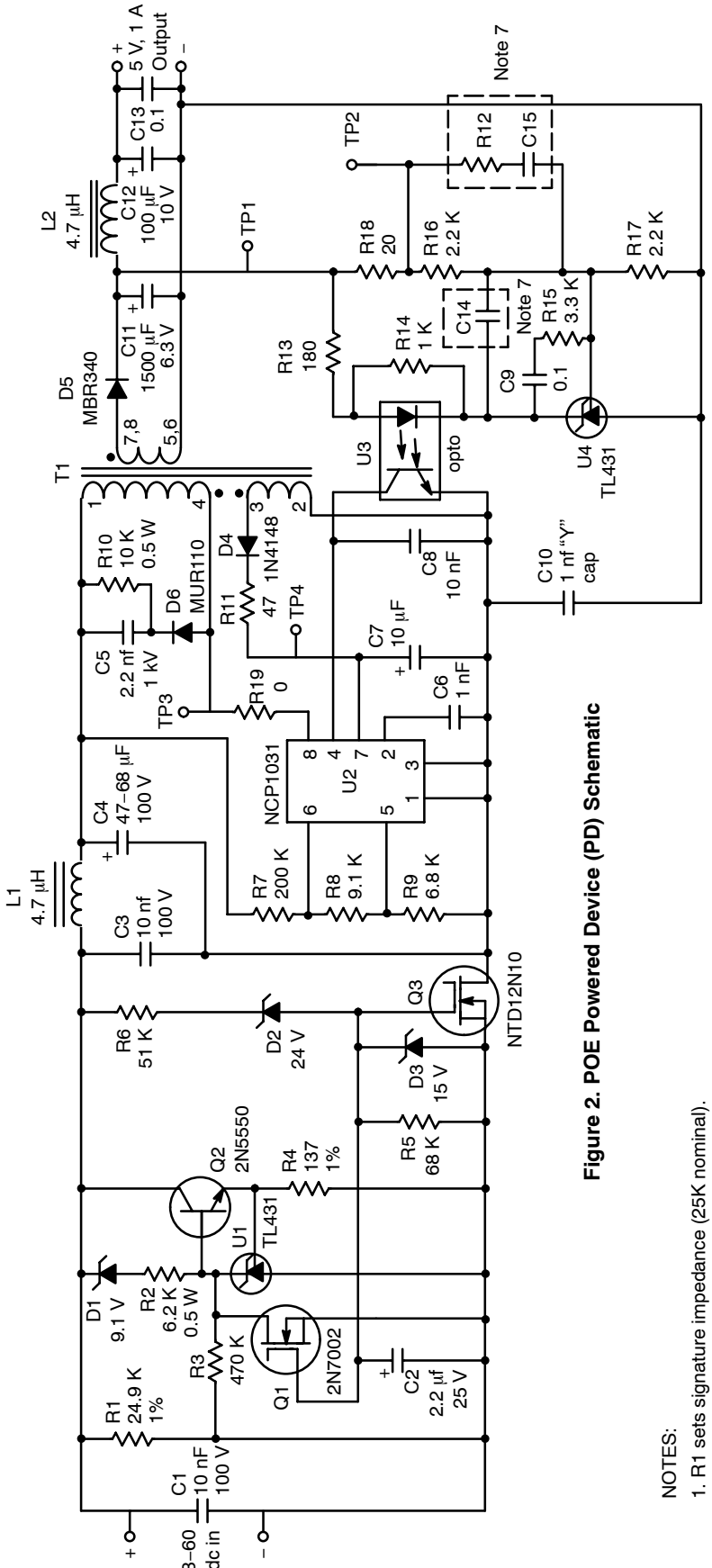



**Figure 2. POE Powered Device (PD) Schematic**

NOTES:

1. R1 sets signature impedance (25K nominal).
2. R4 sets the classification current (18.5 mA nominal for Class 2; 6.5 watts output max).
3. C10 is optional but will improve stability and reduce conducted EMI.
4. R7, R8, & R9 sets converter input UVL and OVP points.
5. C2 sets inrush current profile.
6. Vout set by R16 and R17.
7. Components C14, C15, and R12 required for 6.5 W continuous conduction mode loop stabilization (not necessary for 5.0 W, discontinuous mode operation).
8. Remove R19 to apply current probe wire loop for ID profile monitoring.
9. TP1 and TP2 for signal injection for closed loop analysis.
10. TP3 for NCP1031 internal MOSFET drain voltage monitoring.
11. TP4 for VCC level monitoring.
12. Crossed lines on schematic are not connected.

Part Description: 5 W, 200 kHz POE Flyback Transform, 5 $V_{OUT}$, 48 $V_{IN}$

Schematic ID: T1

Core Type: Ferroxcube EF16 (E16/8/5); 3C95 Material Or Similar

Core Gap: Gap for 100 μH

Inductance: 90 – 100 μH

Bobbin Type: 8 Pin Horizontal Mount for EF16

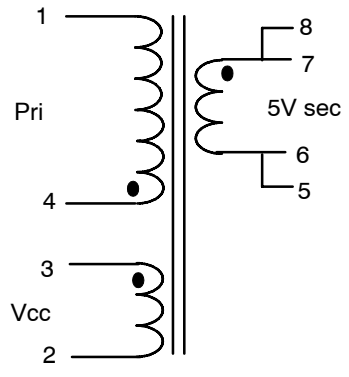
**Windings (in order):**

| **Winding # / Type** | **Turns / Material / Gauge / Insulation Data** |
|---|---|
| $V_{CC}$ / BOOST(2 – 3) | 9 turns of #28HN spiral wound over 1 layer. Insulate with 1 layer of tape (250 V insulation to next winding). |
| Primary(1 – 4) | 24 turns of #28HN over 1 layer. Insulate for 1.5 kV to the next winding. |
| 5 V Secondary (5, 6 – 7, 8) | 4 turns of 4 strands of #28HN flat wound over 1 layer evenly and terminated with 2 strands per pin. Insulate with tape. |

NOTE: Vendor for this transform is Mesa Power Systems (Escondido, CA). Part# 131297.

Hipot: 1.5 kV from $V_{CC}$ Boost/Primary to Secondary.

Schematic




Lead Breakout / Pinout

(Bottom View – facing pins)

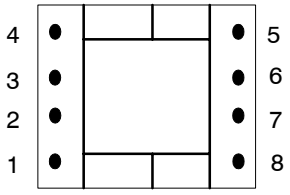



**Figure 3. DCM Flyback Transformer Design**

Part Description: 6.5 W, 220 kHz POE Flyback Transform, 5 $V_{OUT}$, 48 $V_{IN}$

Schematic ID: T1

Core Type: Ferroxcube EF16 (E16/8/5); 3C95 Material Or Similar

Core Gap: Gap for 250 μH

Inductance: 250 ± 15 μH

Bobbin Type: 8 Pin Horizontal Mount for EF16

**Windings (in order):**

| **Winding # / Type** | **Turns / Material / Gauge / Insulation Data** |
|---|---|
| $V_{CC}$ / BOOST(2 – 3) | 18 turns of #28HN spiral wound over 1 layer. Insulate with 1 layer of tape (250 V insulation to next winding). |
| Primary(1 – 4) | 48 turns of #28HN over 2 layer. Insulate for 1.5 kV to the next winding. |
| 5 V Secondary (5, 6 – 7, 8) | 8 turns of 2 strands of #28HN flat wound over 1 layer evenly and terminated with 2 strands per pin. Insulate with tape. |

NOTE: Vendor for this transform is Mesa Power Systems (Escondido, CA). Part# 131294.

Hipot: 1.5 kV from $V_{CC}$ Boost/Primary to Secondary.

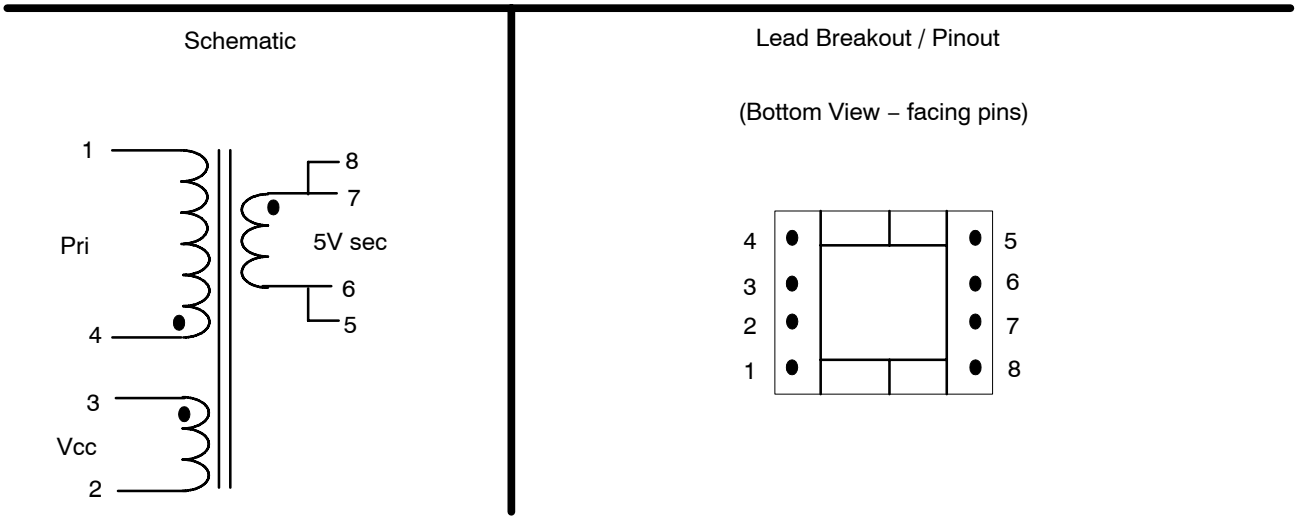



**Figure 4. CCM Flyback Transformer Design**

**Bill of Materials for NCP1031 PoE Demonstration Board**

| Designator | Quantity | Description/Value | Tolerance | Footprint | Manufacturer | Pb−Free |
|---|---|---|---|---|---|---|
| D1 | 1 | MMSZ5239B, 9.1 V Zener | 5% | SOD−123 | ON | YES |
| D6 | 1 | MURS110, 100 V, FR Diode | | SMB | ON | YES |
| D5 | 1 | MBRS340 1 A, 40 V Schottky | | SMC | ON | YES |
| D3 | 1 | MMSZ5245B, 15 V Zener | 5% | SOD−123 | ON | YES |
| D2 | 1 | MMSZ5252B, 24 V Zener | 5% | SOD−123 | ON | YES |
| D4 | 1 | MMSD4148B Diode | | SOD−123 | ON | YES |
| Q2 | 1 | MMBT5550LT, 100 V, NPN Transistor | | SOT−23 | ON | YES |
| Q1 | 1 | 2N7002LT1 MOSFET | | SOT−23 | ON | YES |
| Q3 | 1 | NTD12N10 MOSFET | | DPAK−3 | ON | YES |
| U1, U4 | 2 | TL431AD Programmable Zener | 1% | SOIC−8 | ON | YES |
| U3 | 1 | Optocoupler, SFH6156A−4 (4 Pin) | | Thru Hole (4 pin) | Vishay | YES |
| U2 | 1 | NCP1031DR2G Integrated Controller | | SOIC−8 | ON | YES |
| C10 | 1 | 1 nF ”Y” Cap (Disc Version) | 10% | Thru Hole, LS = 0.25” | Vishay | YES |
| C6 | 1 | 1 nF, 100 V Ceramic Cap | 10% | 0805 | Vishay | YES |
| C8 | 1 | 10 nF, 50 V Ceramic Cap | 10% | 0805 | Vishay | YES |
| C1, C3, | 2 | 10 nF, 100V Ceramic Cap | 10% | 1206 | Vishay | YES |
| C9, C13 | 2 | 0.1 uF, 50 V Ceramic Cap | 10% | 0805 | Vishay | YES |
| C5 | 1 | 2.2 nF, 1 kV Ceramic Cap | 10% | Thru Hole, LS = 0.25” | Vishay | YES |
| C14 | | Not Used | | 0805 | | |
| C15 | | Not Used | | 0805 | | |
| C4 | 1 | 47 or 68 uF, 100 V Electrolytic Cap | 10% | TH, LS = 0.2” or 0.3” | UCC or Rubycon | YES |
| C11 | 1 | 1000 to 1500 uF, 6.3 V Electrolytic Cap | 10% | TH, LS = 0.15” | UCC or Rubycon | YES |
| C12 | 1 | 100 uF, 10 V Min. Electrolytic Cap | 10% | TH, LS = 0.1” | UCC or Rubycon | YES |
| C7 | 1 | 10 uF, 16 V Electrolytic Cap | 10% | TH, LS = 0.1” | UCC or Rubycon | YES |
| C2 | 1 | 1.0 uF to 2.2 uF, 25 V Electrolytic Cap | 10% | TH, LS = 0.1” or 0.15” | UCC or Rubycon | YES |
| R10 | 1 | 10 k, 1/2 W Resistor, 5% | 5% | 2010 | Vishay | YES |
| R2 | 1 | 6.2 k, 1/2 W Resistor, 5% | 5% | 2010 | Vishay | YES |
| R4 | 1 | 137 Ω, 1/8 W, 1% | 1% | 0805 | Vishay | YES |
| R1 | 1 | 24.9 kΩ, 1/8 W, 1% | 1% | 0805 | Vishay | YES |
| R19 | 1 | 0 Ω Resistor | 1% | 1210 | Vishay | YES |
| R18 | 1 | 20 Ω, 1/8 W, 1% | 1% | 0805 | Vishay | YES |
| R11 | 1 | 47 Ω, 1/8 W, 1% | 1% | 0805 | Vishay | YES |
| R13 | 1 | 180 Ω, 1/8 W, 1% | 1% | 0805 | Vishay | YES |
| R14 | 1 | 1 k Ω, 1/8 W, 1% | 1% | 0805 | Vishay | YES |
| R16, R17 | 2 | 2.2 kΩ, 1/8 W, 1% | 1% | 0805 | Vishay | YES |

| Designator | Quantity | Description/Value | Tolerance | Footprint | Manufacturer | Pb–Free |
|---|---|---|---|---|---|---|
| R9 | 1 | 6.8 k, 1/8 W, 1% | 1% | 0805 | Vishay | YES |
| R8 | 1 | 9.1 k, 1/8 W, 1% | 1% | 0805 | Vishay | YES |
| R15 | 1 | 3.3 k, 1/8 W, 1% | 1% | 0805 | Vishay | YES |
| R6 | 1 | 51 k, 1/8 W, 1% | 1% | 0805 | Vishay | YES |
| R5 | 1 | 68 k, 1/8 W, 1% | 1% | 0805 | Vishay | YES |
| R7 | 1 | 200 k, 1/8 W, 1% | 1% | 0805 | Vishay | YES |
| R3 | 1 | 470 k, 1/8 W, 1% | 1% | 0805 | Vishay | YES |
| R12 | | Not Used | | 0805 | | |
| L1, L2 | 2 | Inductor, 4.7 uH, 3 A – PCV–0–472–03 | | TH, LS = 0.4” | Coilcraft | YES |
| T1 | 1 | Transformer, DCM, 5 W<br>Flyback (Custom) – 131297 | | TH<br>(See Figure 3) | Mesa Power Systems | |
| T1 | 1 | Transformer, CCM, 6.5 W<br>Flyback (Custom) – 131294 | | TH<br>(See Figure 4) | Mesa Power Systems | |



**PUBLICATION ORDERING INFORMATION**

**LITERATURE FULFILLMENT**:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
**Phone**: 303–675–2175 or 800–344–3860 Toll Free USA/Canada
**Fax**: 303–675–2176 or 800–344–3867 Toll Free USA/Canada
**Email**: orderlit@onsemi.com

**N. American Technical Support**: 800–282–9855 Toll Free USA/Canada
**Europe, Middle East and Africa Technical Support:**
Phone: 421 33 790 2910
**Japan Customer Focus Center**
Phone: 81–3–5773–3850

**ON Semiconductor Website**: **www.onsemi.com**

**Order Literature**: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative